

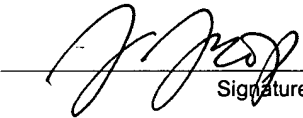


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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) ITL.1046US (P17448)	
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		First Named Inventor Richard E. Fackenthal	
		Art Unit 2133	Examiner Guy J. Lamarre
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.			
This request is being filed with a notice of appeal.			
The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.			
I am the			
<input type="checkbox"/> applicant/inventor.		Signature	
<input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)		Timothy N. Trop Typed or printed name	
<input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>28,994</u>		(713) 468-8880 Telephone number	
<input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____		December 14, 2006 Date	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.			

☒ \*Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	§	
Richard E. Fackenthal	§	Art Unit: 2133
	§	
Serial No.: 10/687,124	§	Examiner: Guy J. Lamarre
	§	
Filed: October 16, 2003	§	Docket: ITL.1046US
	§	P17448
For: Error Correction for Multi-Level Cell Memory with Overwrite Capability	§	Assignee: Intel Corporation
	§	

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Alexandria, VA 22313-1450

**STATEMENT IN SUPPORT OF  
PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Sir:

Claim 1 calls for storing data in a memory array at different densities per cell. Further, it calls for implementing error correction depending on the density of data storage.

The cited reference to Gregori talks about a multi-level memory (ML). He also talks, in the paragraph above Section III on page 752, about the case where ML memories work at variable number of bits per cell. He there explains that the requested error correction capability must be determined for the operating mode with the worst cell error probability (i.e. the operating mode with the highest number of bits per cell). Thus, Gregori is explicit that he does not change the error correction capability depending on the number of bits per cell. Instead, he determines the worst case and sets that as the default regardless of the number of bits per cell. Therefore, clearly, Gregori cannot teach the claimed invention.

Date of Deposit: December 14, 2006

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*Cynthia L. Hayden*  
Cynthia L. Hayden

This is further confirmed in Figure 3 and the material cited on page 754. The input transcoder receives the input c. It also receives a 4-ary/16-ary source word and converts it to a 16-ary source word. The error correction though is not carried out until later, as indicated in the next paragraph. On the basis of the 36 16-ary digit word, the decoder, all the way in the right column of Figure 3, actually does the error coding. All the block with the c input does is convert everything to a 16-ary source word. Thus, the source word is the same regardless of the number of bits per cell. This has no effect on error correction and is simply conforming to a standard value prior to error correction. This is completely consistent with the language previously discussed on page 752. As described earlier, the error correction code simply takes the worst case and applies that across the board.

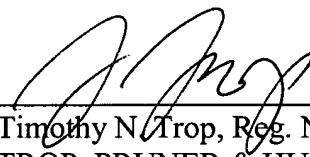
The advisory action misreads the cited material at page 752 which calls for "a" (i.e. one), polyvalent code for a memory operating at two and four bits per cell. This suggests a "one size fits all" approach to error correction.

Therefore, reconsideration is requested with respect to the rejection of claim 1.

On the same basis, reconsideration is requested for the rejection of claim 15. Likewise, reconsideration is requested with respect to claim 29 and claim 38.

Respectfully submitted,

Date: December 14, 2006



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